Design and Optimization of Tunnel FET Device for Low Power VLSI Circuit Applications

SHORT SYNOPSIS

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DOCTOR OF PHILOSOPHY

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by

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CERTIFICATE

I hereby declare that the short synopsis "Design and Optimization of Tunnel FET Device for Low Power VLSI Circuit Applications" being submitted in partial fulfillment of the requirement for the degree of Doctor of Philosophy in Electronics & Communication Engineering under Faculty of Engineering & Technology of Manav Rachna International Institute of Research & Studies, Faridabad during the academic year 2018-2019.

It is a bona fide record of original work carried out under the supervision of Dr. M.K Soni and Dr. Manisha Pattanaik. The work has not been submitted in full or part to any other university or institute for degree or diploma. Further, it is certified that short synopsis is plagiarism free and proof has been submitted.

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ABSTRACT

Tunnel FET device has emerged as a front runner to replace MOSFETs in various low power high performance application circuits. TFET device drew the attention of device designers because of its superior characteristics like: low OFF state current, ability to surpass the 60 mV/decade limitation of subthreshold slope and immunity to short channel effects. In particular Gate All Around TFET (GAATFET) device configuration possess better control of channel electrostatic properties as compared to planar TFET device configuration but its potential for designing analog and digital application circuits has not been explored much in the literature. Optimization with respect to device design parameters of GAATFET device structure will be done for achieving steeper subthreshold slope and improved ON state current which in turn will lead to improved circuit level performance. In this work, circuit analysis of TFET based circuits will be done using a Look Up Table (LUT) based Verilog-A model in SPICE tool. The proposed optimized TFET device structure will be used for designing application circuits like: Amplifier, Ring Oscillator and Static Random Access Memory (SRAM) cell. The performance of TFET based circuits will be compared with the circuits designed using MOSFET device. The research work can be extended further by making use of lower energy band gap material for TFET device fabrication so as to achieve better performance using the proposed TFET device configuration.

Keywords: Band to Band Tunneling, Leakage Power, Subthreshold Slope, High-K Dielectric, Miller Capacitances, Ambipolarity.

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LIST OF ABBREVIATIONS

Symbol	Description
BJT	Bipolar Junction Transistor
BTBT	Band to Band Tunneling
CMOS	Complementary Metal Oxide Semiconductor
CNTFET	Carbon Nano Tube Field Effect Transistors
DGTFET	Double Gate Tunnel Field Effect Transistor
FET	Field Effect Transistor
GAATFET	Gate All Around Tunnel Field Effect Transistor
GNR	Graphene Nano Ribbon
HDTMGTFET	Hetero Dielectric Tri Material Gate Tunnel Field Effect Transistor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PBTI	Positive Bias Temperature Instability
SCE	Short Channel Effect
SPICE	Simulation Program for Integrated Circuit Emphasis
SRAM	Static Random Access Memory
TCAD	Technology Computer Aided Design
TFET	Tunnel Field Effect Transistor
VLSI	Very Large Scale Integration

I. INTRODUCTION

Very Large Scale Integrated (VLSI) circuits industry has witnessed a remarkable improvement in the fabrication process which has enabled the device designers to fabricate chips that have high speed and consumes extremely low power. Electronic circuits in the earlier part of the nineteenth century were dominated by the Vacuum tubes which were developed in 1906. Vacuum tubes had various demerits like: large power consumption, reliability issues, large size and all these shortcomings have made sure that the search for the more efficient and reliable device continued. In 1947, Bardeen, Brattain and Shockley developed first working transistor at Bell's lab and later Bipolar Junction Transistor (BJT) was developed, which remained as a dominant device in the electronics circuit until 1970. Jack Kilby the founder of Texas Instrument came with a big breakthrough when he fabricated the first integrated circuit in the year 1958 by fabricating multiple transistors on a single wafer of silicon. The development at the device level continued and in the year 1959, Kahng & John invented MOSFET in the Bell's lab. Metal Semiconductor Field Effect Transistor (MOSFET) device is based on the patented Field Effect Transistor (FET) proposed by Lilienfield in the year 1925. MOSFET device proved to be more reliable than the bipolar transistor and it also consumes extremely less power as compared to the bipolar transistor. In 1963, Wahlass at Fairchild proposed Complementary Metal Oxide Semiconductor (CMOS) technology which integrates both NMOS and PMOS devices for implementing the desired logic functionality. It is a point to note that most of the modern-day power efficient processors are based on CMOS technology. In 1965, the founder of Intel, Gorden Moore gave a very important law according to which the number of transistors on a chip doubles almost every 18 months. It is popularly known as Moore's law and till now the popular microprocessors from Intel are following this trend.

Complementary Metal Oxide Semiconductor Field Effect Transistor (CMOS) technology that makes use of NMOS and PMOS devices for the implementation of desired logic functionality has dominated the semiconductor manufacturing industry in the last four decades. Nano Scale MOSFET device suffers from various shortcomings like: short channel effects, increased leakage current and poor subthreshold swing which has encouraged the device designers to look for alternative devices which can offer improved performance as compared to MOSFET device. FINFETs, Carbon Nano Tube Field Effect Transistors (CNTFETs) and Tunnel FETs are few of the promising devices which have shown the potential for replacing MOSFET device in the future

VLSI chips. In particular Tunnel FETs have attracted the attention of the device designers primarily because of its inherent property of possessing extremely low leakage current and its ability to surpass the fundamental limit of 60 mV/decade subthreshold swing that is associated with MOSFET device operating at room temperature.

1.1 Power Crisis in VLSI Circuits

VLSI industry has seen tremendous advancement in the fabrication technology over the last four decades and this has ensured that the number of transistors on a chip follows the trend as predicted by Moore's law. Device Scaling has made it possible to achieve high density chips but the extent to which a conventional MOSFET device can be scaled is also limited primarily because of the small geometry effects and the physical limitations imposed by the scaled devices. R. Dennard et al. (1974) proposed a novel technique to scale the MOSFETs keeping the electric field constant. This scaling type is also known as constant field scaling in which all the physical dimensions of the MOSFET device and terminal voltages are scaled by a factor of 1/S, where S represents scaling factor. Source and drain region's doping concentration is increased by a factor of S. The other scaling type is constant voltage scaling in which the terminal voltages are kept constant and the device dimensions are scaled by a factor of 1/S. The doping of source and drain region is increased by a factor of S^2. The scaling techniques impact the device performance and constant field scaling has the advantage of keeping power density unchanged, however this parameter increases by a factor of S^3 in case of constant voltage scaling. This drastic increase in the power density in case of constant voltage scaling can cause serious reliability concerns in the scaled MOSFET device. In most of the practical cases scaling is not performed on all the dimensions of the MOSFET device but a subset of it. Another important point that needs to be considered with device scaling is that it is not possible to scale the device threshold voltage proportionally by the same factor with which the terminal voltages are scaled. This situation is described in Figure 1.1, where it can be seen that with the change in the technology node the threshold voltage (V_T) is not scaled to the large extent as compared to the scaling that is seen in the supply voltage (V_{DD}). This leads to reduced gate overdrive voltage ($V_{OV} = V_{GS}-V_T$) which in turn reduces the I_{ON}/I_{OFF} ratio and also increases propagation delay. This problem which occurs because of reduced gate overdrive voltage can be solved either by reducing the threshold voltage proportionally using some other device engineering technique or by not reducing the supply voltage proportionally with the device dimensions scaling.

In case, the power supply voltage is not reduced proportionally then it will lead to increase in the power dissipation as both leakage power and dynamic power dissipation are related to supply voltage V_{DD} as:

$P_{dynamic} = C_L f V_{DD}^2$

$P_{static} = I_{Leakage} V_{DD}$

Where C_L represents the load capacitance, V_{DD} refers to the supply voltage, f is the average switching frequency and $I_{Leakage}$ is the sum of all the leakage currents in the MOSFET device during the OFF state. Since the dynamic power involves the square of the supply voltage it means that if V_{DD} is not reduced proportionally with the device dimensions then the dynamic power consumption will increase drastically which may lead to heating of the chip ultimately causing permanent damage to it. Subthreshold swing in case of MOSFET is limited to 60 mV/decade at room temperature and various device engineering techniques can be used to improve the subthreshold slope of the device. The improvement in the slope leads to reduction in the device threshold voltage but it also increases the OFF-state current which is evident from Figure 1.2. This increase in the OFF-state current will cause the static power to increase and hence it is a challenging problem because non-proportional scaling of the device threshold voltage increases the static power dissipation.

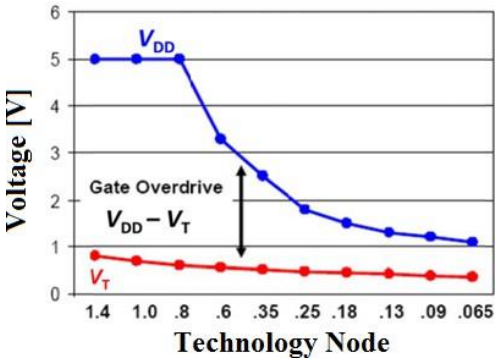

Figure 1.1: V_{DD} & V_T Scaling

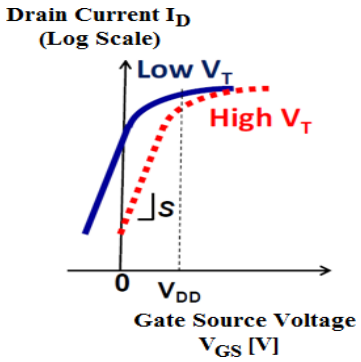

Figure 1.2: Leakage Current increase with steep subthreshold slope

1.2 Steep Subthreshold Swing Devices: Tunnel FET

Tunnel FET has emerged as one of the most promising devices that possess the potential for replacing the conventional MOSFET device for designing low power high performance VLSI circuits. The fundamental limitation of 60 mV/decade subthreshold slope that exist in a MOSFET at room temperature can be surpassed by a TFET device. In order to understand the operating

principle, it becomes extremely important to first compare the TFET device structure with a MOSFET to understand the structural difference between them. Figure 1.3 shows the device structure of n channel MOSFET and NTFET device. Tunnel FET is a P^+-I-N^+ structure with source region P^+ doped, drain region N^+ doped and intrinsic channel region. For the PTFET device the doping of drain and source region will be opposite to that of a NTFET device ie. source has N^+ doping and drain has P^+ doping while the channel region remains intrinsic in both the cases. On the other hand, a conventional n channel MOSFET device consists of source and drain regions as N^+ doped and P^- channel.

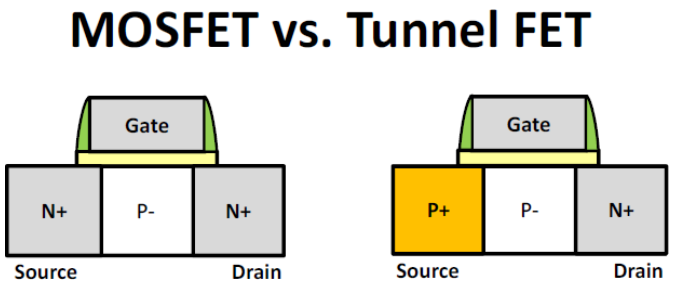

Figure 1.3: Tunnel FET and MOSFET device structure

The Energy band diagram for the tunnel FET device is shown in Figure 1.4. It is clear from Figure 1.4 that during the OFF state (V_{DS}=1V, V_{GS}=0V) the probability of charge carriers crossing the energy barrier is very low and hence the magnitude of the OFF-state current is extremely low, of the order of fA/µm. The prime reason for this low OFF current is that the magnitude of electric field under the influence of which the charge carriers move is very small during the OFF state. When the gate terminal is applied with a positive voltage then the device turns to ON state (V_{GS} = 1V, V_{DS} = 1V) and this results in lowering of the intrinsic region's energy band thereby leading to tunneling of charge carriers from the valence band of the P^+ source to the conduction band of the intrinsic region. The application of the positive gate voltage in case of NTFET device leads to both band bending and band narrowing which ultimately results in the flow of tunneling current. For a MOSFET device in the OFF state (V_{GS} = 0V, V_{DS} = 1V), the energy barrier on the source side p-n junction blocks the thermionic emission of charge carriers. In case of the ON state (V_{GS} = 1V, V_{DS} = 1V) this energy barrier ceases to exist resulting in thermionic emission of charge carriers.

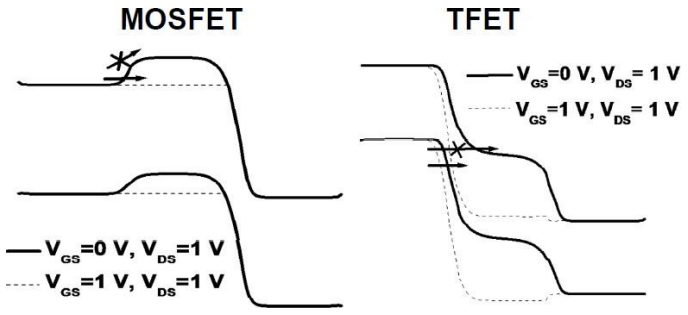

Figure 1.4: Band diagram showing the operating principle of TFET and MOSFET device

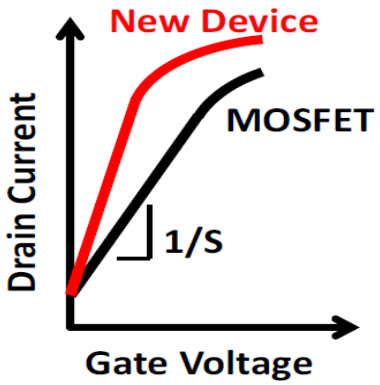

Figure 1.5: Transfer characteristics comparison between MOSFET and Tunnel FET

Figure 1.5 shows the transfer characteristics of Tunnel FET and MOSFET device. It is clear from Figure 1.5 that tunnel FET device exhibits better subthreshold slope as compared to a MOSFET device and also possess low OFF state current which is an inherent advantage of a TFET device that can lead to considerable amount of leakage power saving in VLSI circuits. Despite of all the above-mentioned advantages tunnel FET device also has certain challenges which needs to be addressed and these include: poor ON current, ambipolar conduction and parameter variation effects to name a few.

1.3 Tunnel FET Device Issues and Challenges

Tunnel FET device operates on the phenomenon of energy band gap modulation with the applied gate to source voltage at a constant value of drain source voltage. They possess extremely low OFF state current and it is also clear from the above discussion that these devices can surpass the subthreshold swing limitation of MOSFET device. Despite of all these advantages these devices

suffer from various issues and they must be addressed at the device level itself so as to ensure the reliability of the circuits that will be designed using TFET device. Various issues and challenges that are associated with tunneling devices are discussed below:

1. **Poor ON Current:** Tunnel FET device has inherent advantage of having low OFF state current that has attracted VLSI designers to look at this device as a future device for replacing MOSFET's in low power circuit applications. Despite of having extremely low value of OFF state current, the device also has poor ON current which is 2 to 3 orders smaller than the conventional MOSFET device which is a serious issue and has been addressed by various researchers by modifying the conventional TFET device structure or by changing the material used for device fabrication. The first approach enhances the ON current by increasing the electric field that exists across the source- channel interface resulting in enhanced tunneling probability. The second approach relies on fabricating the TFET device using the semiconductor material which possess lower energy bandgap. Tis approach will be more effective for addressing the ON current issue but at the same time it will also degrade the OFF state current which means that the inherent advantage of low OFF state current in TFET device over the MOSFET device will be lost.

2. **Ambipolar Conduction:** Ambipolar conduction is a severe issue that is associated with Tunnel FET device which ultimately limits its use in digital circuits if not addressed at the device level. TFET device is said to be ambipolar in nature if it conducts current for both higher positive and negative values of the gate voltage. In order to increase the ON state current of the Tunnel FET device, drain doping is kept high but this causes increase in the magnitude of ambipolar current that flows in TFET device. Various device engineering methods have been proposed in the literature to address this problem. One obvious way to counter this issue is to reduce the drain doping which leads to increase in the depletion region width at the drain end and thereby reducing the ambipolar conduction. The only negative point with this technique is that it will impact the ON current of the device.

3. **Miller Effect:** In a tunnel FET, device gate capacitance (Cgg) is a crucial parameter which can have a significant impact on the performance of digital and analog circuits. The total gate capacitance has two parts: Gate source Capacitance (Cgs) and gate drain capacitance

(Cgd). In case of a TFET device maximum contribution to the overall gate capacitance comes from Cgd (also known as Miller Capacitance) and Cgs is extremely small. This is unlike a MOSFET device where Cgs has equal contribution in the overall gate capacitance. Higher magnitude of Miller capacitances in a TFET device can have serious consequences on the performance of digital and analog circuits that makes use of TFET device. For digital circuits, the issue of overshoots and undershoots in the transient simulation and for amplifiers, poor frequency response are very common problems that occurs due to enhanced miller capacitances.

4. **Parameter Variations:** Tunnel FET device like a MOSFET is also prone to variations in the parameters. Be it variations in the physical dimensions of the TFET device or the variation in the threshold voltage caused by random dopant fluctuations, can lead to severe degradation in the tunnel FET device performance. The shrinking of the device dimensions in the nano meter regime has worsened the impact of process variation which results in degraded performance of the device and IC field. Parameter variation comes into picture during fabrication because any fluctuation during fabrication can lead to parameter variations in the device which can shift the device threshold voltage and can cause reliability issues in the VLSI circuits. In order to overcome these issues, techniques at circuit, architecture and process level are required so as to ensure higher yield of IC.

5. **Reliability Concerns:** Degradation of the VLSI circuits performance with time is a major concern for highly scaled silicon technology. In particular for CMOS technology Bias Temperature Stability (BTI) is a serious threat that affects the performance of VLSI circuit with time. In case of tunnel FET device, the traps existing on the channel-dielectric interface (commonly referred to as interface traps) and the traps existing in the dielectric layer (oxide traps) cause the threshold voltage shift causing degradation in the silicon drain current.

II. LITERATURE REVIEW

The discussions made so far has made it clear that tunneling devices have the potential for designing low power VLSI circuits and they possess excellent performance at low supply voltage

that can meet the requirements of designing low power reliable digital and analog circuits. Various researchers have made a significant contribution for improving the performance of Tunnel FET device. Literature review also suggest that these devices have immense potential for deployment in various analog and digital circuits.

Boucart and Ionescu (2007) proposed a novel TFET device structure which has two gates instead of one and it utilizes high-K dielectric material instead of SiO_2. The device simulation result shows that it is capable of achieving high ON state current of 0.23 mA at a gate source voltage of 1.8 V and very low value of OFF state current of approximately 1 fA. Jhaveri, Nagavarapu and Woo (2011) proposed a novel pocket doped structure which was the modified version of the conventional TFET device structure in which an extremely thin N+ layer was inserted at the interface of source and channel region. This device structure resulted in enhancing the ON state current of the Tunnel FET device. Aggarwal, Klimeck and Luisier (2010) proposed a vertical TFET device structure that enhances the ON current by increasing the tunneling area as compared to lateral TFET device.

Anghel, Hraziia, Gupta, Amara and Vladimirescu (2011) proposed a novel technique that can reduce the ambipolar conduction in TFET device keeping the doping concentration of the drain region as high as the doping concentration of the source region. An underlap between gate and drain leads to the reduction in the electric field on the drain side which ultimately results in undesired ambipolar current. Abdi and Kumar (2014) showed that ambipolar conduction can be reduced by introducing an overlap of the gate terminal on drain region. Gate-on-drain overlap TFET device with negative gate voltage will not cause tunnel barrier width narrowing at the interface of drain-channel region, which is the main reason for reduced ambipolar conduction in these oversized TFET device structures.

Cao, Yao, Jiao, Huang, Yu and Li (2011) showed that the degradation in the threshold voltage caused by the interface traps in a Tunnel FET device can be countered by introducing an extremely thin n-layer into the tunneling junction making it a p-n-i-n TFET. Franco, Alian, Vandooren, Verhulst, Linten, Collaert and Thean (2016) investigated the effect of PBTI on the performance of InGaAs TFET's and MOSFET's. The study reveals that sub threshold swing of InGaAs based

TFET device is not much affected as compared to MOSFET under PBTI effect showing the robustness of TFET device against PBTI as compared to MOSFET device. Pocket doped tunnel FET in gate-all-around configuration is also not immune to the interface traps. Madan and Chaujar (2016) showed the effect of the interface traps on the RF/analog performance of the tunnel FET device. Higher donor charge density of the interface traps degrades the OFF state current of the device. Mishra, Narang, Saxena and Gupta (2016) showed that the pocket doped DGTFET device has robust performance under the influence of fixed interface charges ($Si\text{-}SiO_2$) and oxide-oxide interface. Damrongplasit, Kim, Shin and Liu (2013) studied the impact of the RDF in Ge-source TFET's and found that the RDF in the source region has the dominant impact on the variations in the threshold voltage.

Migita, Fukuda, Morita and Ota (2012) showed experimentally that silicon-based tunnel FET device has better temperature stability than a Silicon-based MOSFET device. The fabrication of both these devices was done on the same SOI wafer. Luong, Strangio, Tiedemannn, Lenk, Trellenkamp, Bourdelle, Zhao and Mantl (2016) showed the experimental demonstration of strained silicon nanowire-based Gate All Around NTFET device and inverter circuit for low voltage operation. The major challenge for designing inverter is to design both NTFET and PTFET on the same wafer with similar performance. The experimental results show that strained Si nanowire TFET device possesses higher ON current and excellent analog performance. Chen, Yu, Singh, Shen, Sayanthan, Lo and Kwong (2009) successfully demonstrated the fabrication of vertical silicon nanowire tunnel FET device that achieved steep sub threshold slope of around 70 mV/ decade and an excellent I_{ON} to I_{OFF} current ratio of 10^7.

Mukundrajan, Cotter, Saripalli, Irwin, Datta and Narayanan (2012) proved the potential of using heterojunction TFET device designed using GaSb-InAs semiconductor material for designing ultra-low power circuits. Amir, Trivedi and Mukhopadhyay (2016) demonstrated the implementation of SRAM and eDRAM using Si/Ge TFET device that is designed at 22nm technology node. Mookrejea, Krishnan, Datta and Narayanan (2009) demonstrated the impact of enhanced miller capacitance on the performance of homojunction TFET device-based inverter circuit. Datta, Liu and Narayanan (2014) presented a reliability study of TFET devices and has also shown its impact on the circuit level performance of the SRAM cell. Strangio, Palestri, Esseni,

Selmi and Crupi (2014) successfully demonstrated the robust operation of 6T TFET based SRAM cell that makes use of outward access transistors connecting the internal data storage nodes to the respective bit lines. Lee, Kim, Cai, Lauer, Chang, Koester, Blaauw and Sylvester (2013) explored the opportunity of using Si/SiGe based heterojunction TFET device for designing ring oscillator circuit and SRAM cell.

Ahish, Sharma, Kumar and Vasantha (2016) demonstrated the use of heterojunction TFET device designed using InAs/Si semiconductor material in double gate configuration for the implementation of common source amplifier circuit. Barboni, Siniscalchi and Rodriguez (2015) showed that Graphene Nano Ribbon (GNR) TFETs are most suitable TFET device for designing analog applications which consumes ultra-low power. Roh, Seo, Yoon, Bae, Cho, Lee, Cho and Kang (2014) demonstrated the successful implementation of heterojunction TFET device designed using Ge/GaAs semiconductor material for designing CS amplifier circuit. The TFET device has been designed in gate-all-around configuration. Lu, Paletti, Li, Fay, Ytterdal and Seabaugh (2018) compared the performance of TFET device designed using InAs and GaN semiconductor material with the FinFET device designed at 14 nm technology node for the implementation of common source amplifier and ring oscillator circuit. GaN TFET device based common source amplifier circuit shows extremely high gain of 40.8 dB and consumes extremely low power of 167 pW which is lowest as compared to the CS amplifier implemented using InAs Tunnel FET device and a FinFET device.

2.1 Gaps in Literature

On the basis of exhaustive literature review, certain research gaps have been identified and they are elaborated below:

1. Device scaling has led to power crisis and SCE's, these issues are required to be explored at the device level.
2. Traditional TFET device topologies designed using silicon suffers from poor ON current issue and ambipolarity which limit its use in high performance VLSI circuits.
3. Gate-all-around tunnel FET device topology has better control of channel electrical properties but its potential for both analog and digital applications point of view is still not explored much in the literature.

4. Parameter variation can lead to degradation in the performance of tunnel FET device and this aspect needs to be addressed.
5. Calibrated Verilog-A based model for tunnel FET device is required to perform circuit level simulations involving gate all around tunnel FET devices.
6. Uni-directionality of Tunnel FET's is a challenge for SRAM designing; SRAM circuit topology that ensures reliable read and write operations without changing the conventional topology needs to be explored.

III. DESCRIPTION OF TOPIC

The scaling of the device dimensions leads to increase in the subthreshold leakage current and this has led to significant degradation in the leakage power consumption of the VLSI circuits, ultimately affecting the power budget of VLSI chip. Conventional MOSFET device also suffers from various short channel effects and due to semiconductor/insulator interface trap charges its reliability is becoming a major concern. It has been seen that Tunnel FET device have enormous potential to dominate the IC market and they can be deployed in various analog and digital application circuits as a replacement to the MOSFET device. Tunnel FET offers various advantages like: high I_{ON} to I_{OFF} ratio, steep subthreshold swing, extremely low OFF state current, Immunity to short channel effects and less degradation in the device performance due to the interface trap charges. All these advantages that exists in tunneling devices makes it an ideal device for designing reliable VLSI circuits that operates at low supply voltage.

In spite of the above mentioned merits tunneling devices have various challenges that needs to be addressed. In particular the ON state current of the TFET device needs to be enhanced by using lower energy band gap material for the device fabrication or by making modifications in the device structure. Gate-All-Around TFET (GAATFET) configuration possess better control of the channel electrical characteristics and it is important to explore this device to identify the parameters that can boost its performance and also exploring the potential of the GAATFET device from the point of view of both analog and digital applications. Modeling of the TFET device has been the issue and till date there is no validated compact model available that can be used for simulation of the circuits involving tunneling devices. In order to utilize the look up table-based Verilog-A model for carrying out the circuit level simulations it is extremely important to calibrate the TFET device with reference to the available experimental data.

Tunnel FETs are unidirectional devices and this clearly signifies that it is not possible to interchange source and drain terminals as it is in the case of a MOSFET device. It is also a point to note that mere replacement of the MOSFET device with the tunneling device may lead to incorrect functionality of the circuit. This is a challenging fact for the device designers and they may need to carefully optimize the device sizing of the tunneling transistors used or redesigning of the entire circuit may be needed to ensure correct logic functionality. All the above-mentioned advantages and challenges that are associated with tunneling devices has been the prime motivation to further work on these novel devices after exploring the literature related to Tunnel FET device performance enhancement and its application in various analog and digital circuits. Different topologies of TFET have been analyzed to identify the best topology that can lead to steep subthreshold swing and high I_{ON}/I_{OFF} ratio. The prospects of utilizing the optimized TFET device design in designing power efficient and reliable analog and digital application circuits has also been discussed in detail.

IV. OBJECTIVES OF RESEARCH

The research objectives are framed on the basis of the problems that have been identified by performing exhaustive literature survey done in the area of low power circuit design involving the use of tunneling devices.

4.1 Problem Formulation

Tunneling devices have shown the promise of achieving low power consumption in the standby mode primarily because of its extremely low OFF state current but its performance suffers from poor ON current. Ambipolar conduction, reliability issues and parameter variations also degrade the device performance and hence in order to achieve better circuit level performance a novel TFET device design is needed. Different circuit applications like amplifier, ring oscillator and SRAM cell needs to be explored to prove the potential of the proposed device as a replacement to existing MOSFET device. Circuit level analysis involving tunneling devices is a challenge as validated compact models of TFET device are still not available.

4.2 Objectives

The research work on Design & Optimization of TFET device for low power VLSI circuit applications has been taken up with the following objectives:

1. To perform an exhaustive literature survey in the area of tunnel FET devices.
2. To review the performance of existing TFET device structures and identify the best structures from the point of view of analog and digital applications.
3. To explore the techniques for improving the performance of Tunnel FET devices for deployment in low power and high-performance applications.
4. To investigate gate all around tunnel FET device performance, identify the parameters and perform their optimization for improving the device performance.
5. To design a look up table-based Verilog-A model of Tunnel FET device for performing circuit simulation involving these novel devices.
6. To perform the comparative analysis of ring oscillator circuit designed using CMOS and the proposed HDTMGTFET device.
7. To study and analyze tunnel FET device performance for designing memory (digital) and amplifier (analog) circuits.

V. METHODOLOGY

The objectives mentioned above will be achieved using the following steps:

1. Exhaustive literature survey will be done to gain in depth understanding of the physics behind TFET device and various techniques for optimizing its performance. Survey will also focus on the circuit level applications.
2. Study of the performance of TFET device designed using different semiconductor material (Si, InAs and III-V semiconductors) will be carried out to boost the performance of the TFET device in terms of ON state current and achieving steep subthreshold slope. TFET device structure will be designed in double gate topology and simulations will be done using Genius device simulator where Kane's tunneling model is used using different materials like Si, InAs and III-V semiconductor material. Figure 5.1 shows the workflow used in Genius device simulator.

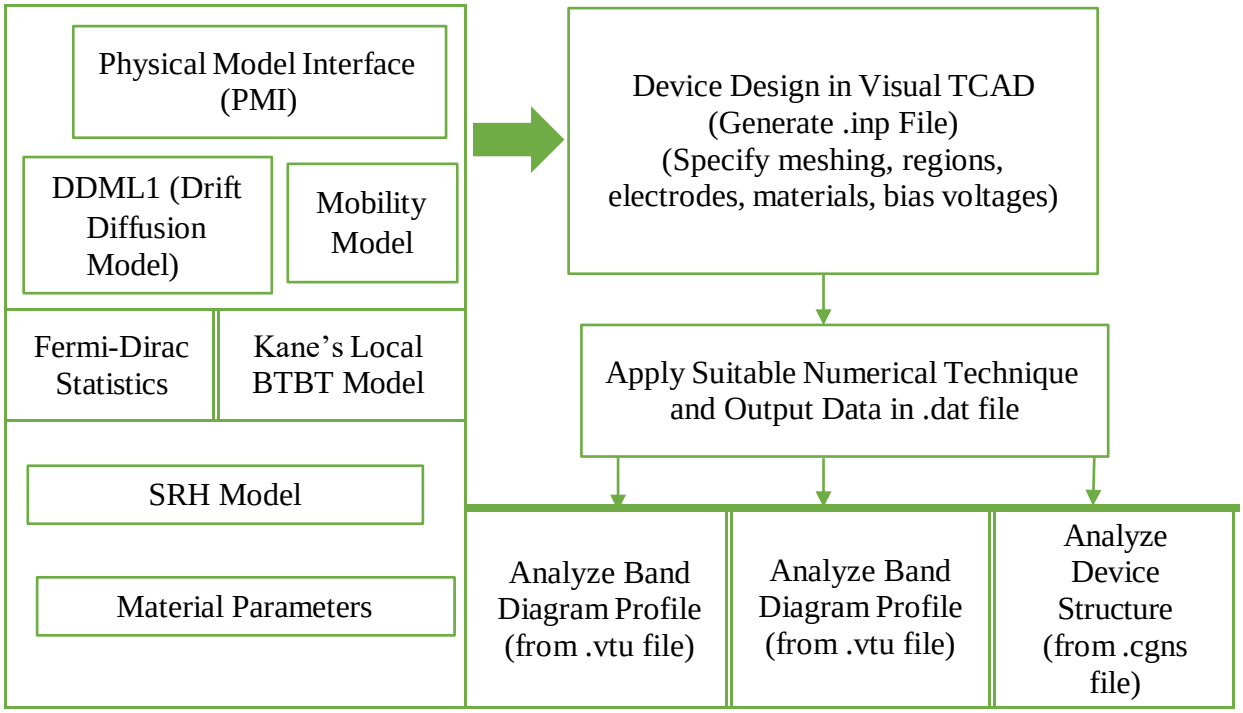
Physical Model Interface (PMI)
DDML1 (Drift Diffusion Model)
Mobility Model
Fermi-Dirac Statistics
Kane's Local BTBT Model
SRH Model
Material Parameters
Device Design in Visual TCAD (Generate .inp File) (Specify meshing, regions, electrodes, materials, bias voltages)
Apply Suitable Numerical Technique and Output Data in .dat file
Analyze Band Diagram Profile (from .vtu file)
Analyze Band Diagram Profile (from .vtu file)
Analyze Device Structure (from .cgns file)

Figure 5.1: Genius Device simulator work flow

3. Optimization of the performance of Gate All Around TFET device configuration will be done by studying the effects of parameter variation on various important performance parameters of GAATFET device. This will involve in depth analysis of variation in the device performance with change in geometrical parameters like: gate oxide thickness, radius of silicon core and drain doping concentration. Optimized set of device sizing parameters and doping concentration will be identified in order to boost the performance of the TFET device designed in gate all around configuration.
4. Designing of look up table based Verilog-A model for performing circuit simulations. This model will be designed by first extracting the current characteristics of the device through dc simulations and capacitance characteristics by carrying out ac simulations on TCAD tool.
5. Comparing the performance of TFET based ring oscillator circuit and amplifier circuit with MOSFET based counterparts. This will make use of the look up table based Verilog A model in SPICE tool and on the other hand, MOSFET device will be simulated using existing PTM models for the same gate length as that of the TFET device. Figure 5.2 shows

the simulation work flow followed for performing circuit simulations involving TFET device.

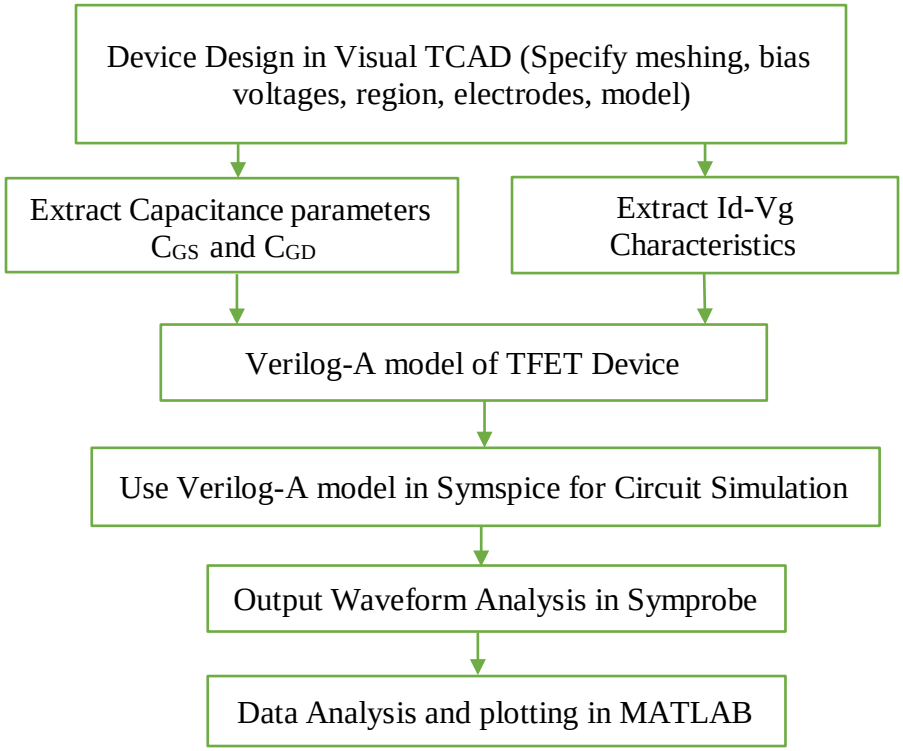
Device Design in Visual TCAD (Specify meshing, bias voltages, region, electrodes, model)
Extract Capacitance parameters C_{GS} and C_{GD}
Extract Id-Vg Characteristics
Verilog-A model of TFET Device
Use Verilog-A model in Symspice for Circuit Simulation
Output Waveform Analysis in Symprobe
Data Analysis and plotting in MATLAB

Figure 5.2: Simulation flow followed

6. Designing a TFET based SRAM cell that can achieve reliable read and write operation and also consumes low power. Detailed investigation will be carried out to analyze the performance of the proposed TFET device structure in SRAM circuit. The parameters that will be considered for analyzing the performance of TFET device in SRAM circuit includes: noise margin, read delay, write delay and number of transistors used.

VI. EXPECTED OUTCOME OF RESEARCH

The research work will explore the possibility to optimize the performance of TFET device and will also explore the prospects of using this device for designing analog and digital circuits. Device performance will be improved in terms of achieving steep subthreshold slope below 60 mV/decade, low OFF state and high ON state current and also ensuring lower ambipolar conduction. The following are the expected outcome of this research work:

1. A novel Tunnel FET device structure will be proposed which will exhibit steep subthreshold slope of less than 60 mV/decade and also possess high ON state current and low OFF state current thereby improving the I_{ON}/I_{OFF} ratio.
2. Parameter variation study will reveal the most significant device parameters that can enhance the performance of the TFET device.
3. A look up table-based Verilog-A model will be designed that can be used in SPICE tool to carry out analysis of TFET based circuits.
4. High gain, low power and wide bandwidth amplifier will be designed to prove the effectiveness of the proposed TFET device in designing analog applications.
5. A low power TFET based ring oscillator circuit will be designed that can achieve sustained oscillations at high output frequency.
6. A low power tunnel FET based SRAM cell will be designed that can achieve reliable read and write operation without much area overhead.

VII. Proposed Time Frame

The research work has been divided into various tasks and each task will be achieved on the basis of the time lines mentioned in the Gannt chart shown below:

8/1/2014
2/17/2015
9/5/2015
3/23/2016
10/9/2016
4/27/2017
11/13/2017
6/1/2018
12/18/2018
7/6/2019
Literature Review Related to Reliability issues in MOSFET & its impact on SRAM
Literature Review Related to Tunnel FET
Literature Review Related to Gate All Around Tunnel FET
TFET Device Designing on TCAD tool
Research Paper on NBTI degradation
Research Paper on Tunnel FET Design and Analysis
Literature Review Related to Analog and Digital Applications of Tunnel FET
Research Paper on GAA TFET optimization
Research Paper on CS Amplifier Design using TFET
Literature Review Related to TFET SRAM Design
Research Paper on SRAM design using TFET
Research Paper on Ring Oscillator Design using TFET
Report Writing

Figure 7.1: Gannt chart of the proposed research work

REFERENCES

Abdi, D.B. and Kumar, M.J., 2014. Controlling ambipolar current in tunneling FETs using overlapping gate-on-drain. *IEEE Journal of the Electron Devices Society*, *2*(6), pp.187-190.

Agarwal, S., Klimeck, G. and Luisier, M., 2010. Leakage-reduction design concepts for low-power vertical tunneling field-effect transistors. *IEEE Electron Device Letters*, *31*(6), pp.621-623.

Ahish, S., Sharma, D., Kumar, Y.B.N. and Vasantha, M.H., 2015. Performance enhancement of novel InAs/Si hetero double-gate tunnel FET using Gaussian doping. *IEEE Transactions on Electron Devices*, *63*(1), pp.288-295.

Amir, M.F., Trivedi, A.R. and Mukhopadhyay, S., 2016. Exploration of Si/Ge tunnel FET bit cells for ultra-low power embedded memory. *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, *6*(2), pp.185-197.

Anghel, C., Gupta, A., Amara, A. and Vladimirescu, A., 2011. 30-nm tunnel FET with improved performance and reduced ambipolar current. *IEEE Transactions on Electron Devices*, *58*(6), pp.1649-1654.

Barboni, L., Siniscalchi, M., & Sensale-Rodriguez, B., 2015. TFET-based circuit design using the transconductance generation efficiency gm/Id method. *IEEE Journal of the Electron Devices Society*, *3*(3), 208–216.

Boucart, K., & Ionescu, A. M., 2007. Double-gate tunnel FET with high-κ gate dielectric. *IEEE Transactions on Electron Devices*, *54*(7), 1725–1733.

Cao, W., Yao, C.J., Jiao, G.F., Huang, D., Yu, H.Y. and Li, M.F., 2011. Improvement in reliability of tunneling field-effect transistor with pnin structure. *IEEE Transactions on Electron Devices*, *58*(7), pp.2122-2126.

Chen, Z.X., Yu, H.Y., Singh, N., Shen, N.S., Sayanthan, R.D., Lo, G.Q. and Kwong, D.L., 2009. Demonstration of tunneling FETs based on highly scalable vertical silicon nanowires. *IEEE Electron Device Letters*, *30*(7), pp.754-756.

Damrongplasit, N., Kim, S.H., Shin, C. and Liu, T.J.K., 2013. Impact of gate line-edge roughness (LER) versus random dopant fluctuations (RDF) on germanium-source tunnel FET performance. *IEEE Transactions on Nanotechnology*, *12*(6), pp.1061-1067.

Datta, S., Liu, H. and Narayanan, V., 2014. Tunnel FET technology: A reliability perspective. *Microelectronics Reliability*, *54*(5), pp.861-874.

Franco, J., Alian, A., Vandooren, A., Verhulst, A.S., Linten, D., Collaert, N. and Thean, A., 2016. Intrinsic robustness of TFET subthreshold swing to interface and oxide traps: A comparative PBTI study of InGaAs TFETs and MOSFETs. *IEEE Electron Device Letters*, *37*(8), pp.1055-1058.

Jhaveri, R., Nagavarapu, V. and Woo, J.C., 2010. Effect of pocket doping and annealing schemes on the source-pocket tunnel field-effect transistor. *IEEE Transactions on Electron Devices*, *58*(1), pp.80-86.

Lee, Y., Kim, D., Cai, J., Lauer, I., Chang, L., Koester, S.J., Blaauw, D. and Sylvester, D., 2013. Low-power circuit analysis and design based on heterojunction tunneling transistors (HETTs). *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, *21*(9), pp.1632-1643.

Lu, H., Paletti, P., Li, W., Fay, P., Ytterdal, T. and Seabaugh, A., 2018. Tunnel FET Analog Benchmarking and Circuit Design. *IEEE Journal on Exploratory Solid-State Computational Devices and Circuits*, *4*(1), pp.19-25.

Luong, G.V., Strangio, S., Tiedemannn, A., Lenk, S., Trellenkamp, S., Bourdelle, K.K., Zhao, Q.T. and Mantl, S., 2016. Experimental demonstration of strained Si nanowire GAA n-TFETs and inverter operation with complementary TFET logic at low supply voltages. *Solid-State Electronics*, *115*, pp.152-159.

Madan, J. and Chaujar, R., 2016. Interfacial charge analysis of heterogeneous gate dielectric-gate all around-tunnel FET for improved device reliability. *IEEE Transactions on Device and Materials Reliability*, *16*(2), pp.227-234.

Migita, S., Fukuda, K., Morita, Y. and Ota, H., 2012, June. Experimental demonstration of temperature stability of Si-tunnel FET over Si-MOSFET. In *2012 IEEE Silicon Nanoelectronics Workshop (SNW)* (pp. 1-2). IEEE.

Mishra, A., Narang, R., Saxena, M. and Gupta, M., 2016. Impact of Interfacial Fixed Charges on the Electrical Characteristics of Pocket-Doped Double-Gate Tunnel FET. *IEEE Transactions on Device and Materials Reliability*, *16*(2), pp.117-122.

Mookerjea, S., Krishnan, R., Datta, S. and Narayanan, V., 2009. Effective capacitance and drive current for tunnel FET (TFET) CV/I estimation. *IEEE Transactions on Electron Devices*, *56*(9), pp.2092-2098.

Mukundrajan, R., Cotter, M., Saripalli, V., Irwin, M.J., Datta, S. and Narayanan, V., 2012, August. Ultra low power circuit design using tunnel FETs. In *2012 IEEE Computer Society Annual Symposium on VLSI* (pp. 153-158). IEEE.

Roh, H.B., Seo, J.H., Yoon, Y.J., Bae, J.H., Cho, E.S., Lee, J.H., Cho, S. and Kang, I.M., 2014. Evaluation of Radio-Frequency Performance of Gate-All-Around Ge/GaAs Heterojunction Tunneling Field-Effect Transistor with Hetero-Gate-Dielectric by Mixed-Mode Simulation. *Journal of Electrical Engineering & Technology, 9(6),* pp.2070-2078.

Strangio, S., Palestri, P., Esseni, D., Selmi, L. and Crupi, F., 2014, June. Performance analysis of different SRAM cell topologies employing tunnel-FETs. In *72nd Device Research Conference* (pp. 143-144). IEEE.

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